Laboratory 4

(Due date: **002/003**: March 9th, **004**: March 10th, **006**: March 11th)

OBJECTIVES

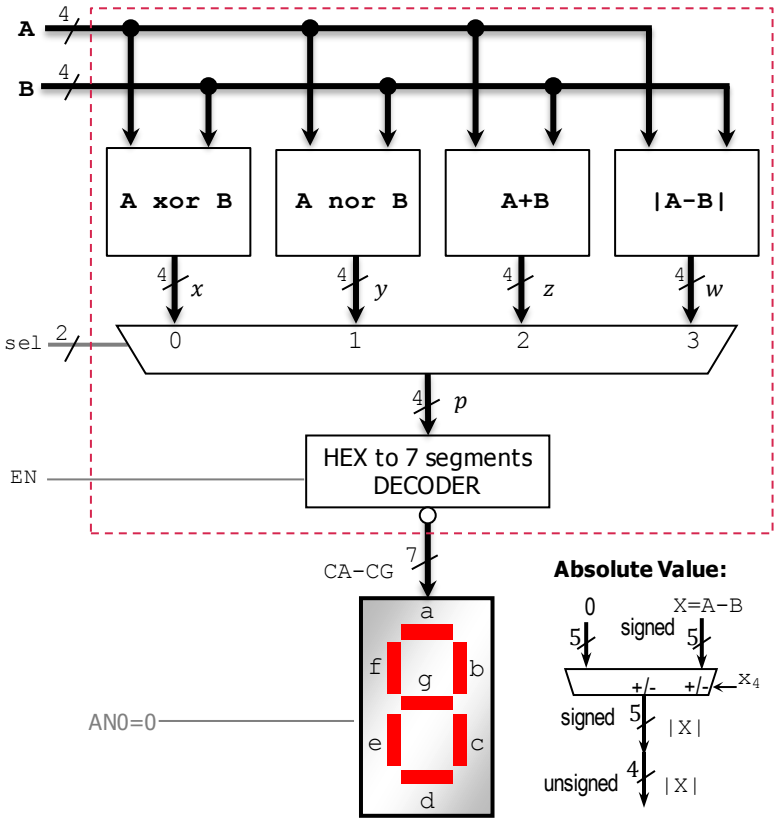
- ✓ Use the Concurrent Description and the Structural Description in VHDL.
- ✓ Implement Combinational circuits on an FPGA.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

FIRST ACTIVITY: (100/100)

- **SIMPLE 4-BIT ARITHMETIC LOGIC UNIT (ALU):** This circuit selects between arithmetic (absolute value, addition) and logical (XOR, NOR) operations. Only one result (hexadecimal value) can be shown on the 7-segment display. This is selected by the input `sel(1..0)`.
- Arithmetic operations: The 4-bit inputs `A` and `B` are treated as unsigned numbers.
  - ✓ `A+B`: If there is a carry out, ignore it.
  - ✓ `|A-B|`: 4-bit result, since `|A-B|` ∈ [0,15]. Tip: zero-extend the inputs to 5 bits and implement `A-B` (5-bit signed result). Then, implement `|A-B|`, where the 5-bit signed result is always positive. Finally, use the magnitude (4 LSBs) as the unsigned output.
- Logic Operations (`A xor B, A nor B`): These are bit-wise operations.
- HEX to 7 segments decoder:
  - ✓ If `EN=1` → Decoder is enabled. Result appears on the 7-segment display.
  - ✓ If `EN=0` → Decoder is disabled. All LEDs in the 7-segment display need to be off.
- **Nexys-4 A7 and Basys 3**: Each 7-segment display has active-low inputs (`CA-CG`) and an active-low enable `AN`. Make sure that only one 7-segment display is activated (e.g.: In Nexys 4, to use only the right-most 7-segment display, set `AN0=0`, `AN1-AN7=1`).



- **VIVADO DESIGN FLOW FOR FPGAs – NEXYS A7-50T**
  - ✓ Create a new Vivado Project. Select the **XC7A50T-1CSG324 Artix-7 FPGA** device.
  - ✓ Write the VHDL code for the given circuit. Synthesize your circuit to clear syntax errors. Pay attention to the warnings.
    - **IMPORTANT**: For `A+B` and `|A-B|` circuits, you must use full adders and logic gates (as in Lab 2).
    - To implement the Bus MUX and decoder, it is strongly advised that you use the VHDL concurrent statements. To implement the top file, use the Structural Description: Create a separate file for the Arithmetic and Logic circuits, the 4-to-1 Bus MUX, and the Hex to 7-segment decoder (with active low outputs).
  - ✓ Write the VHDL testbench to simulate the circuit. Use 8 sets of `A` and `B` values. For each set, make `sel` vary from 0 to 3. Also, include a case (e.g.: `A = 0001, B = 1001, sel=11`) with `EN=0` to verify that the 7-segment display is OFF (`CA-CG = 1111111`). Here is an example for one set of `A` and `B` values:
    - `A = 0001, B = 1001, sel = 00, EN = 1`
    - `A = 0001, B = 1001, sel = 01, EN = 1`
    - `A = 0001, B = 1001, sel = 10, EN = 1`
    - `A = 0001, B = 1001, sel = 11, EN = 1`
    - `A = 0001, B = 1001, sel = 11, EN = 0`

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- ✓ Perform Behavioral Simulation and Timing Simulation of your design. **Demonstrate this to your TA**.
  - Behavioral Simulation: Add internal signals (x, y, z, w, p) to the waveform view. Go to: SCOPE window: testbench → UUT. Then go to Objects Window → Signal(s) → Add to Wave Window. Finally, re-run the simulation.

    - This step is extremely useful when debugging your circuit. Your circuit might be cleared of syntax errors, but there might still be errors that can be difficult to spot. By tracing the internal signals, we can determine where the error is located in the circuit.

    - For example: In this circuit, for a given set of input values, we can compute the expected output values and internal signal values. Then, we compare those values with those provided by the simulation:
      If the output `CA-CG` is incorrect (simulation results do not match our calculated values), we then look at the value of the signal p:
      - If the value of p is correct (i.e., simulation results match our calculated values), then the error is in the HEX to 7-segments Decoder.
      - If the value of p is incorrect, then look at the values of x, y, z, w. If all of them are correct, then the error is in the Bus MUX. If any of the values of x, y, z, w are incorrect, then we can determine which arithmetic or logic unit is generating incorrect output values.

  - For the following set of inputs, complete the expected values of the listed internal signal and outputs. Then, run the simulation and compare the values in the simulation waveform with the ones you computed. This will help you figure out where the errors (if any) are located at.

A	**B**	x	y	z	w	sel	EN	p	CA-CG
0001	1001					00	1		
						01			
						10			
						11			
1000	0010					00	1		
						01			
						10			
						11			

- ✓ I/O Assignment: Create the XDC file. Nexys A7-50T: Use `SW0` to `SW7` for the inputs `A` and `B`, `SW8` to `SW10` for the inputs `sel` and `EN`, `CA-CG` (7-segment display signals), and `AN7-AN0` (anode enable for each 7-segment display).
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) all the generated files: VHDL code files, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____ **Date:** _____